19-1291; Rev 0; 9/97

MAXIM

IF Undersampler

General Description

The MAX1005 is a combined digitizer and reconstruction integrated circuit designed to work in systems that demodulate and modulate communications signals. It integrates IF undersampling and signal synthesis functions into a single, low-power circuit. Its analog-to-digital converter (ADC) is used to directly sample or undersample a downconverted RF signal, while its digital-to-analog converter (DAC) recreates the IF subcarrier and transmission data. The MAX1005's ADC is ideal for undersampling applications, due to the analog input amplifier's wide (15MHz) bandwidth. The DAC has very low glitch energy, which minimizes the transmission of unwanted spurious signals. An on-chip reference provides for low-noise ADC and DAC conversions.

The MAX1005 provides a high level of signal integrity from a low power budget. It operates from a single power supply, or from separate analog and digital supplies with independent voltages ranging from +2.7V to +5.5V. The MAX1005 can operate with an unregulated analog supply of 5.5V and a regulated digital supply down to 2.7V. This flexible power-supply operation saves additional power in complex digital systems.

The MAX1005 has three operating modes: transmit (DAC active), receive (ADC active), and shutdown (ADC and DAC inactive). In shutdown mode, the total supply current drops below 1µA. The device requires only 2.4µs to wake up from shutdown mode. The MAX1005 is ideal for hand-held, as well as base-station applications. It is available in a tiny 16-pin QSOP package specified for operation over both the commercial and extended temperature ranges.

Applications

PWT1900

PHS/P

Wireless Loops

PCS/N

Functional Diagram appears at end of data sheet.

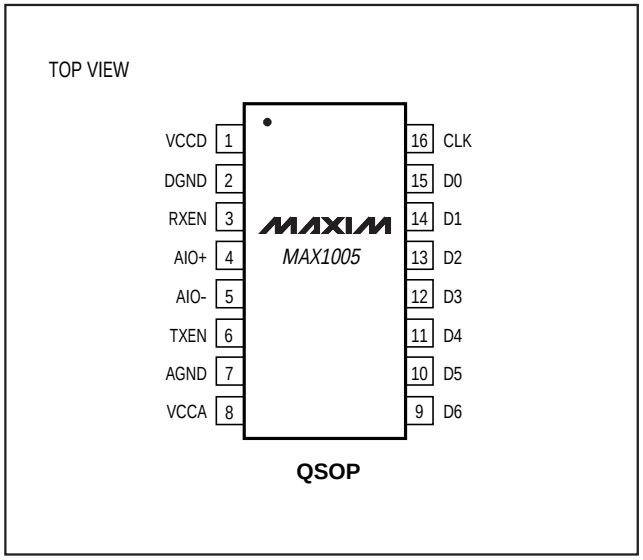
Features

- ♦ **Differential-Input, 5-Bit ADC**
- ♦ **Differential-Output, 7-Bit DAC**
- ♦ **15Msps Min Conversion Rate**
- ♦ **25MHz -1dB Full-Power Bandwidth**
- ♦ **44dB SFDR for ADC**
  39dB at 10.7MHz SFDR (Imaged) for DAC
- ♦ **Internal Voltage Reference**
- ♦ **Parallel Logic Interface**
- ♦ **Single-Supply Operation (+2.7V to +5.5V)**
- ♦ **0.1µA Low-Power Shutdown Mode**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1005CEE	0°C to +70°C	16 QSOP
MAX1005EEE	-40°C to +85°C	16 QSOP

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

VCCA to AGND .....-0.3V, +6.0V
VCCD to DGND .....-0.3V, +6.0V
VCCA to VCCD .....±6.3V
Digital I/O Pins (D0–D6, CLK, RXEN, TXEN)
to DGND .....-0.3V to (VCCD + 0.3V) or 6.0V (whichever is smaller)
Analog I/O Pins (AIO+, AIO-)
to AGND.....(VCCA - 1.5V) to (VCCA + 0.3V)
AGND to DGND.....-0.3V, +0.3V

Power Dissipation (T_A = +70°C)
QSOP (derate 5.90mW/°C above 70°C) 470mW
Operating Temperature Ranges
MAX1005CEE .....0°C to +70°C
MAX1005EEE.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, <10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCCA = VCCD = 3.0V, f_{CLK} = 15MHz, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMIT DAC DC ACCURACY (Note 1)							
Resolution	N			7			Bits
Integral Nonlinearity	INL				±0.2	±1	LSB
Differential Nonlinearity	DNL				±0.2	±1	LSB
Offset Error						±1	LSB
Transmit Full-Scale Output Voltage	V_{OUT}			736	800	864	mVp-p
TRANSMIT DAC DYNAMIC PERFORMANCE (T_A = +25°C) (Note 2)							
Spurious-Free Dynamic Range	SFDR	(Note 3)	VCCA = VCCD = 3.0V	28	39		dBc
			VCCA = VCCD = 2.7V to 5.5V		39		
Total Harmonic Distortion plus Noise	THD+N	(Note 4)	VCCA = VCCD = 3.0V			-28	dBc
Wakeup Time Exiting Shutdown	t_{WAKE}				0.7	2.4	µs
Clock Feedthrough		(Note 5)			-50		dBc
DAC Latency		(Notes 6, 7)				0.5	CLK period
Power-Supply Rejection	PSR	VCC_ (A or D or both) = 3.0V ±100mVp-p at 100kHz			67		dB
TRANSMIT ADC DC ACCURACY (Note 8)							
Resolution	N			5			Bits
Integral Nonlinearity	INL				±0.2		LSB
Differential Nonlinearity	DNL				±0.2		LSB
Offset Error		AIO+ = AIO-			±2		LSB
Full-Scale Input Range	V_{IN}			368	400	432	mV
RECEIVE ADC DYNAMIC PERFORMANCE (T_A = +25°C) (Note 8)							
Total Harmonic Distortion	THD	(Notes 9, 10)	VCCA = VCCD = 3.0V		-42	-24	dB
			VCCA = VCCD = 2.7V to 5.5V		-42		
Spurious-Free Dynamic Range	SFDR	(Note 9)	VCCA = VCCD = 3.0V	24	44		dB
			VCCA = VCCD = 2.7V to 5.5V		44		
Effective Number of Bits	ENOB	(Note 9)	VCCA = VCCD = 3.0V	4.5	4.9		Bits
			VCCA = VCCD = 2.7V to 5.5V		4.9		

ELECTRICAL CHARACTERISTICS (continued)

(VCCA = VCCD = 3.0V, f_{CLK} = 15MHz, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Full-Power Bandwidth (-1dB)		V_{IN} = 90% of full scale		15	25		MHz
Conversion Rate				15			Msps
Wakeup Time Exiting Shutdown Mode	t_{WAKE}				0.6	2.4	µs
Power-Supply Rejection	PSR	VCC_ (A or D or both) = 3.0V ±100mVp-p at 100kHz			<0.1		LSB
ANALOG INPUT/OUTPUT (AIO+, AIO-) (Note 11)							
Input Resistance	R_{IN}	T_A = +25°C, differential between AIO+ and AIO-		1.56	2.00	2.44	kΩ
Input Resistance Temperature Coefficient	TCR_{IN}				-2000		ppm/°C
Input Capacitance (Note 6)	C_{IN}	Differential between AIO+ and AIO-				4	pF
		AIO+ or AIO- to GND				4	
POWER REQUIREMENTS							
Supply Voltage	VCCA, VCCD			2.7		5.5	V
Analog Supply Current	ICCA	VCCA = VCCD = 3.0V, C_L ≤ 12.5pF	RXEN = 1, TXEN = 0, ADC on, DAC off		9.0	14.8	mA
			RXEN = 0, TXEN = 1, ADC off, DAC on		2.5	3.8	
Digital Supply Current	ICCD	VCCA = VCCD = 3.0V, C_L ≤ 12.5pF	RXEN = 1, TXEN = 0, ADC on, DAC off		4.0	6.4	mA
			RXEN = 0, TXEN = 1, ADC off, DAC on		3.0	5.6	
Shutdown Supply Current	ICCA + ICD	VCCA = VCCD = 3.0V, C_L ≤ 12.5pF, RXEN = TXEN			<0.1	5	µA
DIGITAL INPUTS/OUTPUTS (D0–D6, RXEN, TXEN, CLK) (Note 12)							
Output High Voltage	V_{OH}	D0–D4, VCCD = 2.7V to 5.5V, I_{SOURCE} = 200µA		VCCD - 1.0		VCCD	V
Output Low Voltage	V_{OL}	D0–D4, VCCD = 2.7V to 5.5V, I_{SINK} = 50µA		0		0.5	V
Input High Voltage	V_{IH}	VCCD = 2.7V to 5.5V	D0–D6, CLK	0.7VCCD			V
			RXEN, TXEN	VCCD - 0.5		VCCD + 0.1	
Input Low Voltage	V_{IL}	VCCD = 2.7V to 5.5V	D0–D6, CLK			0.3VCCD	V
			RXEN, TXEN	-0.1		0.5	

ELECTRICAL CHARACTERISTICS (continued)

(VCCA = VCCD = 3.0V, f_{CLK} = 15MHz, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current	I_{IN}	D0–D6, CLK; VCCD = 2.7V to 5.5V		-1		7	µA
		RXEN, TXEN; VCCD = 2.7V to 3.6V	TXEN = RXEN			±1	
			TXEN = 0 and RXEN = 1, or TXEN = 1 and RXEN = 0			±2	
		RXEN, TXEN; VCCD = 3.6V to 5.5V	TXEN = RXEN			±1	
			TXEN = 0 and RXEN = 1, or TXEN = 1 and RXEN = 0			±4	
Input Capacitance	C_{IN}	D0–D6, CLK; TXEN = 1, RXEN = 0 (Note 6)				8	pF
TIMING CHARACTERISTICS (Data Outputs: R_L = 1MΩ, C_L = 15pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 12)							
DAC Data Setup Time	t_{DS}	T_A = +25°C (Note 6)		5	0.6		ns
DAC Data Hold Time	t_{HOLD}	T_A = +25°C (Note 6)		5	0.3		ns
CLK Duty Cycle				45		55	%
ADC CLK to Output Data Valid	t_{DO}	C_L ≤ 12.5pF			13	20	ns

Note 1: TXEN = 1, RXEN = 0. All DAC transfer function parameters are measured differentially from AIO+ to AIO- using the End-Point Linearity method.

Note 2: f_{IN} = 4.3MHz digital sine wave applied to DAC data inputs; f_{CLK} = 15MHz. The reference frequency (f_{REF}) is defined to be 10.7MHz (f_{CLK} - f_{IN}). All frequency components present in the DAC output waveform except for f_{REF} and f_{IN} are considered spurious.

Note 3: For DAC SFDR measurements, the amplitude of f_{REF} (10.7MHz) is compared to the amplitudes of all frequency components of the output waveform except for f_{IN} (4.3MHz).

Note 4: For DAC measurements, THD+N is defined as the ratio of the square-root of the sum-of-the-squares of the RMS values of all harmonic and noise components of the output waveform (except for f_{IN} and f_{REF}) to the RMS amplitude of the f_{REF} component.

Note 5: Clock feedthrough is defined as the difference in amplitude between the f_{REF} component and the f_{CLK} component when measured differentially from AIO+ to AIO-.

Note 6: Guaranteed by design. Not production tested.

Note 7: The DAC input interface is a master/slave register. An additional half clock cycle is required for data at the digital inputs to propagate through to the DAC switches.

Note 8: RXEN = 1, TXEN = 0. Unless otherwise noted, for all receive ADC measurements, the analog input signal is applied differentially from AIO+ to AIO-, specified using the Best-Fit Straight-Line Linearity method.

Note 9: f_{IN} = 10.7MHz, f_{CLK} = 15MHz. Amplitude is 1dB below full-scale. The reference frequency (f_{REF}) is defined to be 4.3MHz (f_{CLK} - f_{IN}). All components except for f_{REF} and f_{IN} are considered spurious.

Note 10: Receive ADC THD measurements include the first five harmonics.

Note 11: CAUTION: Operation of the analog inputs AIO+ and AIO- (pins 4 and 5) at more than 1.5V below VCCA could cause latchup and possible destruction of the part. Avoid shunt capacitances to GND on these pins. If shunt capacitances are required, then bypass these pins only to VCCA.

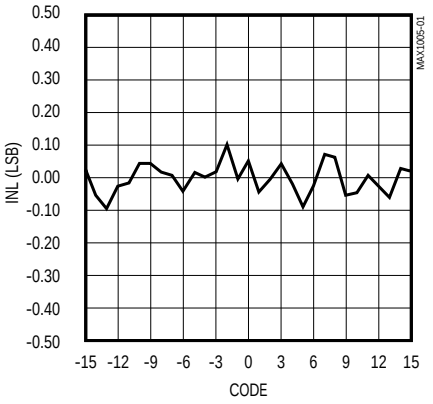
Note 12: All digital input signals are measured from 50% amplitude reference points. All digital output signal propagation delays are measured to $V_{OH(AC)}$ for rising output signals and to $V_{OL(AC)}$ for falling output signals. The values for $V_{OH(AC)}$ and $V_{OL(AC)}$ as a function of the VCCD supply are shown in the following table:

VCCD (V)	$V_{OH(AC)}$ (V)	$V_{OL(AC)}$ (V)
2.7 to 3.3	VCCD - 1.1	0.5
3.3 to 5.5	2/3 x VCCD	0.5

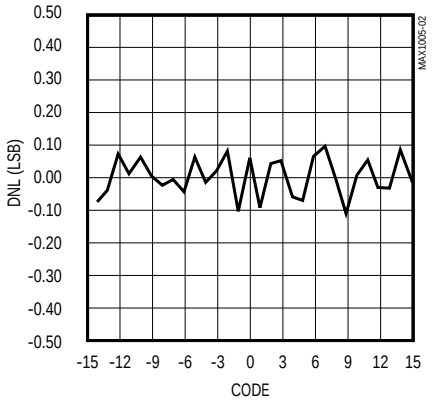
Typical Operating Characteristics

(VCCA = VCCD = 3.0V, T_A = +25°C, unless otherwise noted.)

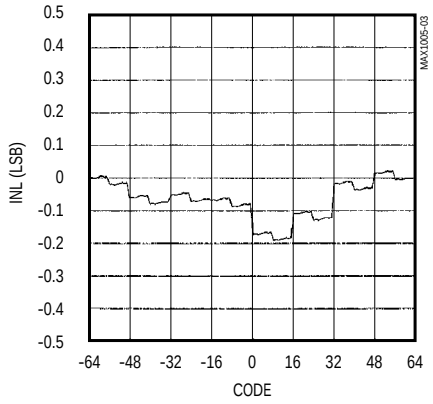
RECEIVE ADC INTEGRAL NONLINEARITY



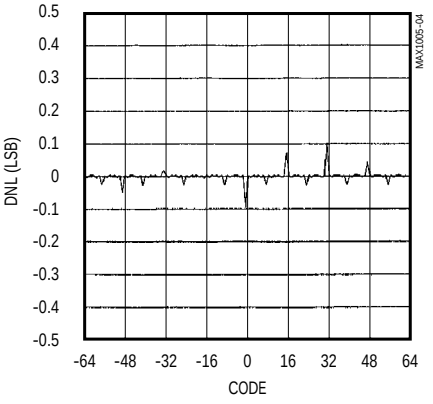
RECEIVE ADC DIFFERENTIAL NONLINEARITY



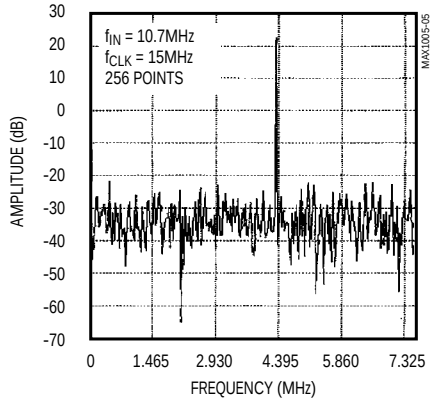
TRANSMIT DAC INTEGRAL NONLINEARITY



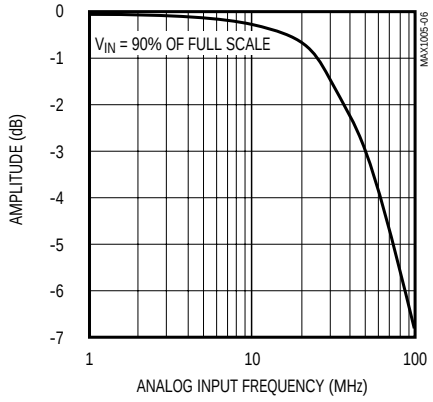
TRANSMIT DAC DIFFERENTIAL NONLINEARITY



RECEIVE ADC FFT PLOT



FULL POWER ANALOG INPUT BANDWIDTH



Pin Description

PIN	NAME	FUNCTION
1	VCCD	Digital Supply Voltage, +2.7V to +5.5V
2	DGND	Digital Ground. Connect to digital ground plane.
3	RXEN	Receive ADC Enable Input. A logic-high level on this input combined with a logic-low level on TXEN enables the receive ADC and disables the transmit DAC. If RXEN = TXEN, the MAX1005 enters its low-power shutdown mode.
4	AIO+	Positive Analog Input/Output Pin. If RXEN = 1 and TXEN = 0, then AIO+ is the positive analog input to the receive ADC. If RXEN = 0 and TXEN = 1, then AIO+ is the positive transmit DAC output pin.
5	AIO-	Negative Analog Input/Output Pin. If RXEN = 1 and TXEN = 0, then AIO- is the negative analog input to the receive ADC. If RXEN = 0 and TXEN = 1, then AIO- is the negative transmit DAC output pin.
6	TXEN	Transmit DAC Enable Input. A logic-high level on this input combined with a logic-low level on RXEN enables the transmit DAC and disables the receive ADC. If RXEN = TXEN, the MAX1005 enters its low-power shutdown mode.
7	AGND	Analog Ground. Connect to analog ground plane.
8	VCCA	Analog Supply Voltage, +2.7V to +5.5V
9, 10	D6, D5	Two MSBs for DAC input data. D6 is the MSB.
11–15	D4–D0	Data Input/Output Pins. If RXEN = 0 and TXEN = 1, then D4–D0 function as the five lower bits of DAC input data, with D0 as the LSB. If RXEN = 1 and TXEN = 0, then D4–D0 function as the five data outputs for the ADC, with D4 as the MSB and D0 as the LSB. In low-power shutdown mode (RXEN = TXEN), D0–D4 should not be externally held high, to prevent excessive input leakage currents.
16	CLK	Clock Input. If the receive ADC is active (RXEN = 1, TXEN = 0), the analog input is sampled on the falling edge of clock and the data outputs (D4-D0) are updated on the rising edge of CLK. If the transmit DAC is active (TXEN = 1, RXEN = 0), input data is clocked in on the falling edge of CLK and the DAC output is updated on the rising edge of CLK. The input clock may continue to run when the MAX1005 is shut down (TXEN = RXEN).

Detailed Description

The MAX1005 is designed to operate with the Maxim PWT1900 (TAG-6) wireless transceiver chipset consisting of the MAX2411 RF transceiver, the MAX2511 IF transceiver, and the MAX1007 power-control/diversity IC. The MAX1005 integrates all the functions of an IF undersampler into a single low-power integrated circuit. It is also well suited for other time-division duplex (TDD) communications systems. This device includes a 7-bit transmit DAC, a 5-bit receive ADC, two internal bandgap references, clock drivers, and all necessary interface and control logic.

Transmit DAC

The low-side alias frequency (f_{CLK} - f_{OUT} = 10.7MHz) generated by the MAX1005's 7-bit DAC is used to recreate the IF sub-carrier and transmission data in TDD and other communications systems. The DAC accepts CMOS input data in the twos-complement format and outputs a corresponding analog voltage differentially between AIO+ and AIO-. The full-scale output voltage range is typically ±400mV. The DAC code table is shown in Table 1.

Table 1. Transmit DAC Code Table

DAC INPUT DATA	ANALOG OUTPUT
011 1111	+FS
000 0000	0
100 0000	-FS

Receive ADC

The 5-bit receive ADC is used to directly sample or undersample a downconverted RF signal. The ADC converts an analog input signal to a 5-bit digital output code in the twos-complement format. Figure 1 shows the ADC transfer function.

Analog input signals are applied differentially between AIO+ and AIO-, with a full-scale range of ±200mV. An internal amplifier buffers the input signal and drives the comparator array, minimizing loading on the external signal source. The input amplifier has a full-power -1dB bandwidth of at least 15MHz, making this device ideally suited for undersampling applications.

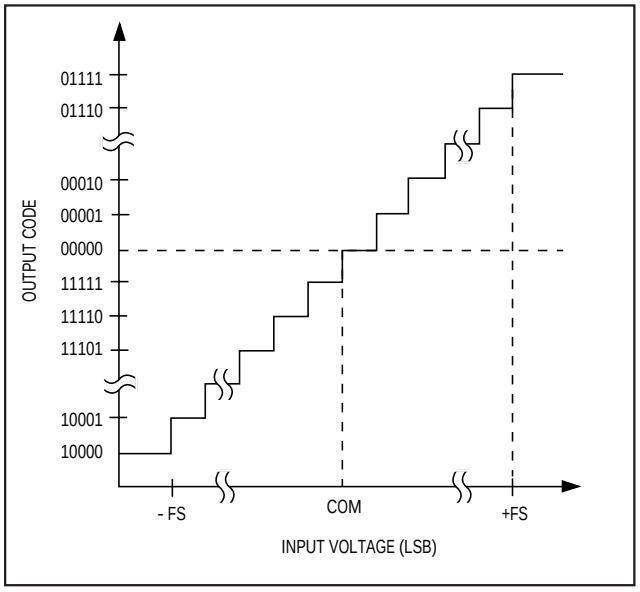


Figure 1. Receive ADC Transfer Function

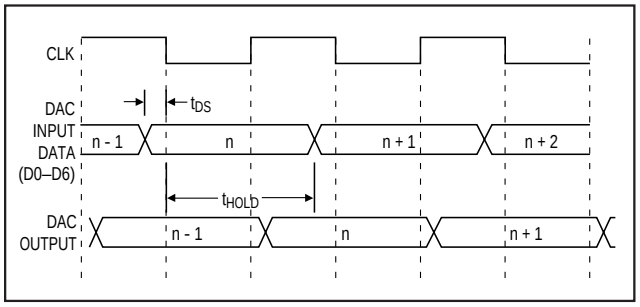


Figure 2. Transmit DAC Timing Diagram

Digital Interface

The DAC has a 7-bit parallel digital interface. Figure 2 shows the timing diagram for the transmit DAC. Digital data is latched into the DAC input register on the falling edge of CLK. On the next rising edge of CLK the data is transferred to the DAC register and the DAC output voltage is updated.

The ADC is enabled by setting TXEN = 0 and RXEN = 1. Figure 3 shows the ADC timing diagram. Input data is sampled on the falling edge of CLK, while output data changes state on the rising edge of CLK. This minimizes digital feedthrough and noise while the analog input is being sampled. The ADC output data is applied to the 5-bit parallel output pins (D0–D4), with the MSB at D4.

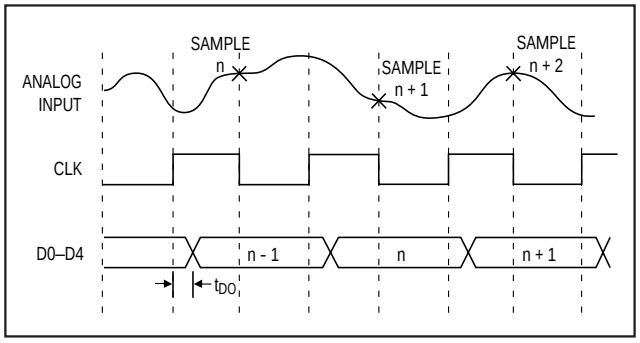


Figure 3. Receive ADC Timing Diagram

Operating Modes

The MAX1005 has three operating modes: transmit, receive, and shutdown. The operating mode is selected by the RXEN and TXEN inputs, as shown in Table 2.

In transmit mode, the DAC is active and the ADC is inactive. Power consumption is typically 16.5mW with a 3V supply voltage. In receive mode, the ADC is active and the DAC is inactive. Power consumption in this mode is typically 39mW with a 3V supply voltage.

The third mode is shutdown, in which both the DAC and the ADC are inactive. Select this mode by setting RXEN = TXEN at any voltage from DGND to VCCD. In shutdown mode, the CLK input can continue to run without damaging the device and with no significant increase in the typical shutdown supply current specification of 0.1µA. When exiting shutdown, the MAX1005 is guaranteed to be operational within 2.4µs after TXEN or RXEN is asserted, as shown in Table 2.

To prevent supply-current drain due to leakage currents from entering the ADC output bits, the ADC outputs (D0–D4) should not be held high in low-power shutdown mode.

Table 2. Operating Mode Selection

RXEN	TXEN	OPERATING MODE
0	0	Low-power shutdown: ADC and DAC disabled
0	1	Transmit mode: DAC active, ADC disabled
1	0	Receive mode: ADC active, DAC disabled
1	1	Low-power shutdown: ADC and DAC disabled

IF Undersampler

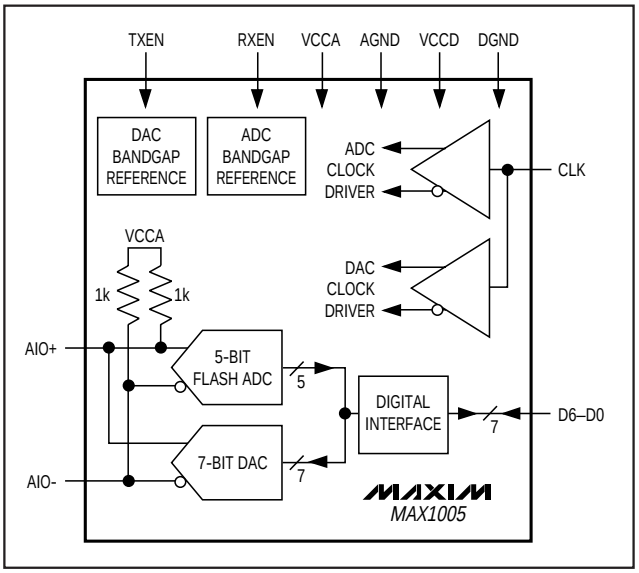
Power-Supply Bypassing and Grounding

The MAX1005 has separate analog (VCCA) and digital (VCCD) power-supply connections, as well as separate analog and digital ground connections to minimize coupling of noisy digital signals into the circuit's analog portion. The device will operate with both of these power supplies connected to any voltage between +2.7V and +5.5V. This feature allows the digital circuitry to operate from a regulated logic power supply; this reduces power consumption and maintains compatibility with external logic, while allowing the analog circuitry to operate from an unregulated supply.

The analog ground (AGND) and digital ground (DGND) should be tied together close to the device. At no time should the voltage between AGND and DGND exceed ±0.3V.

The entire board needs good DC bypassing for both analog and digital supplies. Place the power-supply bypass capacitors close to where the power is routed onto board. 10µF electrolytic capacitors with low equivalent-series-resistance (ESR) ratings are recommended. For best effective bits performance, minimize capacitive loading at the digital outputs. Keep the digital output traces as short as possible. Bypass each of the VCC_ supply pins to its respective GND with high-quality ceramic capacitors located as close to the package as possible.

Functional Diagram

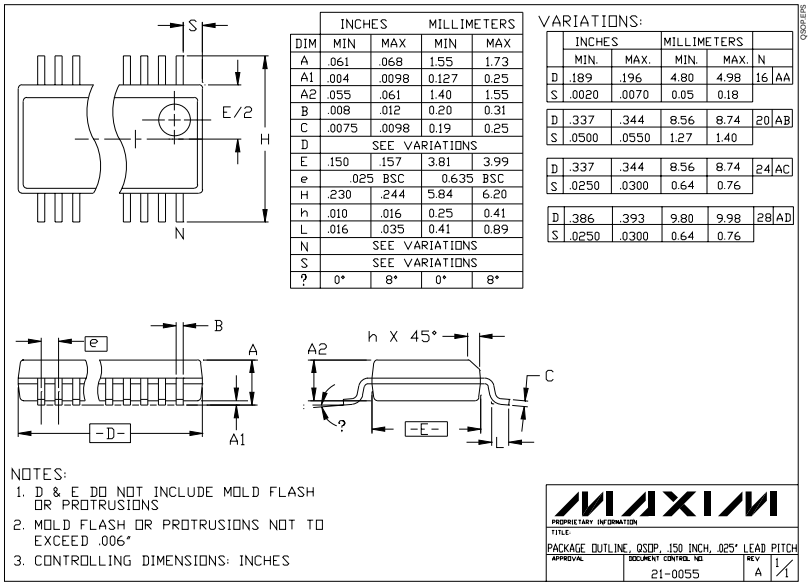


Chip Information

TRANSISTOR COUNT: 2377

SUBSTRATE CONNECTED TO AGND

Package Information



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.127	0.25
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.19	0.25
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
S	SEE VARIATIONS			
?	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.27	1.40		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.64	0.76		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.64	0.76		